JSPM's
RAJARSHI SHAHU COLLEGE OF ENGINEERING
TATHAWADE, PUNE-33
(An Autonomous Institute Affiliated to Savitribai Phule Pune University,Pune)

Department of Electronics and Telecommunication Engineering

Structure

(2025 Pattern)

W.e.f. 2025-26

Department of Electronics and Telecommunication Engineering

Vision

"To create an educational environment to meet the challenges of modern Electronics and Telecommunication engineering industry through state of art technical knowledge and

Mission

- To entrust the students with fundamentals of Electronics and Telecommunication Engineering for successful carrier
- To enable students to pursue higher education, research and promote Entrepreneurship
- To serve the nation through techno-social development.

Dr. S. C. Wagaj
B.O.S. Chairman

Dr. A. M. Badadhe
Dean Academics

J.S.P.M.'s Rajarshi Shahu College of Engineering Pune University I.D. No. PU/PN/Engg./173/(2001) Tathawade, Pune-33

Dr. S. P. Bhosle
Director RSCOE, Pune

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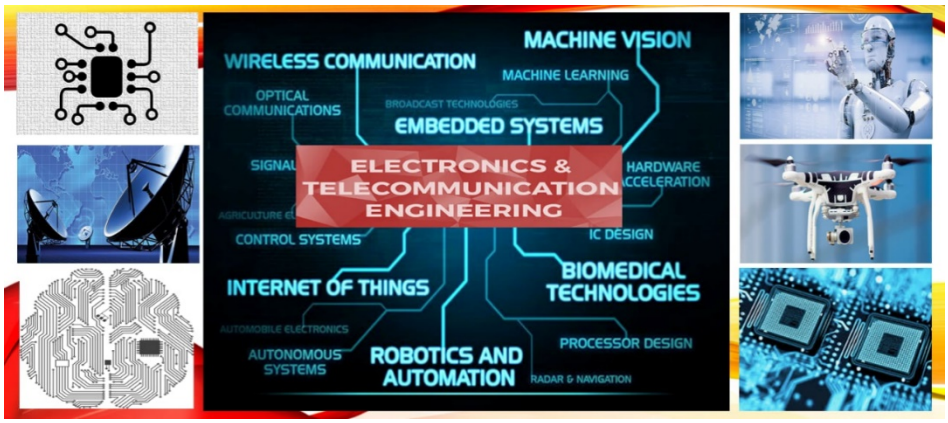

Program Outcomes (POs)

Engineering Post graduates will be able to:

1. Independently carry out research/investigation and development work to solve practical problems.
2. Write and present a substantial technical report/document.
3. Demonstrate degree of mastery over the area as per the specialization of the program.
4. Acknowledge the responsibility to contribute for sustainable development of society.
5. Engage in lifelong learning, inculcating professional practices and ethics.

Highlights of the Syllabus

Curriculum of Electronics and Telecommunication Engineering course is designed in consultation with

The salient features of curriculum designed in association with **KPIT, Nayan Electronics and Matrix automations.**

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Unique features of the curriculum

1. **Curriculum centered at Outcome Based Education:**

   The new Curriculum is based on student-centered instruction models that focus on measuring student performance through outcomes. The outcomes include subject knowledge, industry required skills and attitudes.

2. **Emphasize on Advanced courses:**

   The nature of the new curriculum is rigorous and well prescribed so that the students can spend more time on preparation and self-study. This will benefit them to grasp and get expertise in the most effective

   Creativity and Innovation:

   Along with experiential learning, the curriculum also motivates the students to inculcate creativity and innovation. Apart from conventional lab, the curriculum provides a freedom for students to perform industry assignments, pilot projects, innovative development, etc.

3. **Three Tracks in M-Tech:** The curriculum provides three tracks in the curriculum as

   I. VLSI II. Embedded System

4. **Industry Induced Internship Program** To support ever demanding industry requirements, the curriculum has included an industry internship with an objective to learn technologies pertaining to their discipline and enhance their technical knowledge with a support of the live platform of Industry.

5. **Motivation for Self Learning:**

   The curriculum also offers a freedom to students to take the initiatives in their learning needs and set the goals with the help of online learning platforms like MOOCs, NPTEL, Swayam, etc.

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F Y. M. Tech (VLSI & Embedded system)
Semester -I (2025 Pattern)

Course Code	Course	Teaching Scheme			Examination Scheme					Credits
		TH	TU	PR	ISE (20)	MSE (30)	ESE 50)	TW	TOTAL	TOTAL
EC5301T	Digital CMOS Design	3	--	--	20	30	50	--	100	3
EC5302T	Embedded System Design	3	--	--	20	30	50	--	100	3
EC5303T	Research Methodology and Intellectual Property Rights	3	--	--	20	30	50	--	100	3
EC5304T	Elective-I	3	--	--	20	30	50	--	100	3
EC5305T	Elective-II	3	--	--	20	30	50	--	100	3
EC5306L	Lab Practice I	--	--	4	ISCE--60		40		100	2
EC5307L	Lab Practice II	--	--	2	ISCE--30		20		50	1
EC5308L	Online course Certification	--	--	4	ISCE--60		40		100	2
EC5309	Audit Course	Non credit								
Total		**15**	**--**	**10**					**750**	**20**

Elective-I		Elective-II	
Code No.	**Title**	**Code No.**	**Title**
EC5304T- A	Advanced Device Physics	EC5305T- A	System Design Through Verilog
EC5304T- B	Embedded Automotive System	EC5305T- B	Embedded Product Design

Name of Audit Courses			
Code No.	**Title**	**Code No.**	**Title**
EC5309	Technical Paper writing	ME5208	Value Education In Engineering
CE5208	Disaster Management	CS5209	Constitution of India

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F. Y. M. Tech. (VLSI& Embedded Systems)
Semester-II (2025 Pattern)

Course Code	Course	Teaching Scheme			Examination Scheme					Credits
		TH	TU	PR	ISE (20)	MSE (30)	ESE (50)	TW	TOTAL	TOTAL
EC5310T	Analog CMOS Design	3	--	--	20	30	50	--	100	3
EC5311T	Embedded Signal Processor Architecture	3	--	--	20	30	50	--	100	3
ES5204T	Advance Engineering Mathematics	3	--	--	20	30	50	--	100	3
EC5312T	Elective-III	3	--	--	20	30	50	--	100	3
EC5313T	Elective-IV	3	--	--	20	30	50	--	100	3
EC5314L	Lab Practice III	--	--	4	ISCE--60		40	-	100	2
EC5315L	Lab Practice IV	--	--	2	ISCE--30		20	-	50	1
EC5316L	Seminar	-	-	4	ISCE--60		40	-	100	2
Total		**15**	**--**	**10**					**750**	**20**

Elective-III		Elective-IV	
Code No.	**Title**	**Code No.**	**Title**
EC5312T-A	Nano Electronics	EC5313T-A	Display Material and Technologies
EC5312T-B	Artificial Intelligence and Machine Learning	EC5313T-B	Industrial IoT

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